What Is Claimed Is:

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1. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

a trench formed into a surface of the substrate;

first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a channel region therebetween, wherein the second region is formed underneath the trench, and the channel region includes a first portion that extends substantially along a sidewall of the trench and a second portion that extends substantially along the surface of the substrate;

an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region and a portion of the first region; and

an electrically conductive control gate having a first portion disposed in the trench.

2. The device of claim 1, wherein the control gate has a second portion disposed over and insulated from the floating gate.

3. The device of claim 2, wherein the control gate forms a notch at a connection between the control gate first portion and the control gate second portion.

4. The device of claim 3, wherein the floating gate includes a sharp edge that extends toward the notch.

5. The device of claim 1, wherein the floating gate is disposed over the entire second portion of the channel region.

6. The device of claim 1, wherein the floating gate is insulated from the control gate by an insulation layer having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

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7. The device of claim 2, further comprising:

a layer of insulating material formed along sidewalls of the trench and extending between the control gate and the floating gate.

8. The device of claim 7, wherein the layer of insulating material includes:

a first portion formed along sidewalls of the trench and between the control gate and the channel region first portion; and

a second portion formed under the control gate and over the floating gate.

9. The device of claim 1, wherein channel region first portion extends in a direction directly toward the floating gate.

10. The device of claim 1, wherein the trench has a side wall with an indentation formed therein, and wherein the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

11. The device of claim 1, wherein:

the trench has a side wall with an indentation formed therein,

the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, and

the floating gate is disposed over and insulated from a second part of the channel region second portion.

12. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

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a plurality of trenches formed into a surface of the substrate which are substantially parallel to one another and extend across the isolation and active regions in a second direction that is substantially perpendicular to the first direction;

each of the active regions including a plurality of memory cells extending in the first direction, each of the memory cells comprising:

first and second spaced-apart regions formed in the substrate having a second conductivity type, with a channel region formed in the substrate therebetween, wherein the second region is formed underneath one of the trenches, and wherein the channel region has a first portion extending substantially along a sidewall of the one trench and a second portion extending substantially along the surface of the substrate, and

an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region and a portion of the first region; and

a plurality of electrically conductive control gates each extending along one of the active regions, wherein the control gates each have first portions disposed in the trenches.

13. The array of claim 12, wherein the control gates each have second portions disposed over and insulated from the floating gates

14. The array of claim 13, wherein the control gates form notches at points where the control gate first and the second portions meet.

15. The array of claim 14, wherein the floating gates include sharp edges that extend toward the notches.

16. The array of claim 12, further comprising:

a layer of isolation material extending along each of the isolation regions and filling portions of the trenches that are in the isolation regions.

17. The array of claim 16, wherein the isolation material layer in each of the isolation regions is disposed between a pair of the control gates in adjacent active regions.

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18. The array of claim 12, wherein for each of the memory cells, the floating gate is disposed over the entire second portion of the channel region.

19. The array of claim 12, wherein for each of the memory cells, the floating gate is insulated from the control gate by an insulation layer having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

20. The array of claim 13, wherein each of the memory cells further comprises a layer of insulating material formed along sidewalls of the trench and extending between the control gate and the floating gate.

21. The array of claim 20, wherein the layer of insulating material for each memory cell includes:

a first portion formed along sidewalls of the trench and between the control gate and the channel region first portion; and

a second portion formed under the control gate and over the floating gate.

22. The array of claim 12, further comprising a plurality of conductive contacts each electrically connected to one of the first regions.

23. The array of claim 12, further comprising a plurality of conductive contacts each electrically connected to one of the second regions.

24. The array of claim 12, wherein each of the channel region first portions extend in a direction directly toward one of the floating gates.

25. The array of claim 12, wherein the memory cells are formed as pairs of memory cells, and wherein each of the memory cell pairs share a single second region therebetween.

26. The array of claim 12, wherein for each of the memory cells, the trench has a side wall with an indentation formed therein, and the control gate first portion includes a protruding

portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

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27. The array of claim 12 wherein for each of the memory cells:

the trench has a side wall with an indentation formed therein,

the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, and

the floating gate is disposed over and insulated from a second part of the channel region second portion.

28. The array of claim 12 wherein the second regions are integrally formed together in one of a plurality of conductive lines buried in the substrate, and wherein each of the conductive lines extends in the second direction and includes a raised portion that extends up to the substrate surface.

29. A method of forming a semiconductor memory cell, comprising the steps of:

forming a first region in a semiconductor substrate, wherein the substrate has a first conductivity type and the first region has a second conductivity type;

forming a trench into a surface of the semiconductor substrate, wherein the trench is spaced apart from the first region;

forming a second region in the substrate and underneath the trench, wherein the second region has the second conductivity type and a channel region in the substrate is defined between the first and second regions, the channel region includes a first portion that extends substantially along a sidewall of the trench and a second portion that extends substantially along the substrate surface;

forming a floating gate of electrically conductive material disposed over and insulated from at least a portion of the channel region and a portion of the first region; and

forming a control gate of electrically conductive material having a first portion disposed in the trench.

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30. The method of claim 29, wherein the control gate has a second portion disposed over and insulated from the floating gate.

31. The method of claim 30, wherein the control gate forms a notch at a connection between the control gate first portion and the control gate second portion.

32. The method of claim 31, wherein the floating gate includes a sharp edge that extends toward the notch.

33. The method of claim 29, wherein the floating gate is disposed over the entire second portion of the channel region.

34. The method of claim 29, further comprising the step of:

forming a layer of insulation material between the floating gate and the control gate that has a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

35. The method of claim 30, further comprising the step of:

forming a layer of insulating material that extends along sidewalls of the trench and between the control gate and the floating gate.

36. The method of claim 35, wherein the formation of the layer of insulating material includes the steps of:

forming a first portion of the layer of insulating material along sidewalls of the trench and between the control gate first portion and the channel region first portion; and

forming a second portion of the layer of insulating material under the control gate second portion and over the floating gate.

37. The method of claim 29, wherein channel region first portion extends in a direction directly toward the floating gate.

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38. The method of claim 29, wherein the formation of the floating gate includes forming a layer of the electrically conductive material before the formation of the trench, and wherein the trench is subsequently formed through a portion of the layer of electrically conductive material.

39. The method of claim 29, further including the step of:

forming an indentation in a sidewall of the trench so that the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of the floating gate.

40. The method of claim 29, further including the step of:

forming an indentation in a sidewall of the trench so that the control gate first portion includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of the channel region second portion, wherein the floating gate is disposed over and insulated from a second part of the channel region second portion.

41. A method of forming an array of semiconductor memory cells, comprising the steps of:

forming a plurality of first regions in a semiconductor substrate that are substantially parallel to one another and extend in a first direction, wherein the substrate has a first conductivity type and the first regions have a second conductivity type;

forming a plurality of trenches into a surface of the semiconductor substrate, wherein the trenches are spaced apart from and extend substantially parallel to the first regions;

forming a plurality of second regions in the substrate having the second conductivity type and are substantially parallel to one another, each of the second regions extends in the first direction and is formed underneath one of the trenches, wherein a plurality of channel regions in the substrate are defined each having a first portion extending substantially along a sidewall of one of the trenches and a second portion that extends substantially along the substrate surface between the one trench and one of the first regions;

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forming a plurality of floating gates of electrically conductive material each disposed over and insulated from at least a portion of one of the channel regions and a portion of one of the first regions; and

forming a plurality of control gates of electrically conductive material each having a first portion disposed in one of the trenches.

42. The method of claim 41, further comprising the steps of:

forming spaced apart isolation regions on the semiconductor substrate which are substantially parallel to one another and extend in a second direction substantially orthogonal to the first direction, with an active region between each pair of adjacent isolation regions; and

forming insulating material in portions of the trenches that are in the isolation regions.

43. The method of claim 41, wherein the control gates each have a second portion disposed over and insulated from one of the floating gates.

44. The method of claim 43, wherein for each of the active regions, the control gate second portions therein are electrically connected together.

45. The method of claim 43, wherein each of the control gates form a notch at a connection between its control gate first portion and its control gate second portion.

46. The method of claim 45, wherein each of the floating gates include a sharp edge that extends toward one of the notches.

47. The method of claim 41, wherein each of the floating gates is disposed over the entire second portion of one of the channel regions.

48. The method of claim 41, further comprising the step of:

forming a layer of insulation material between each of the floating gates and one of the control gates having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

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49. The method of claim 43, further comprising the step of:

forming insulating material that extends along sidewalls of the trenches and between the control gates and the floating gates.

50. The method of claim 49, wherein the formation of the insulating material includes the steps of:

forming first portions of the insulating material along sidewalls of the trenches and between the control gate first portions and the channel region first portions; and

forming second portions of the insulating material under the control gate second portions and over the floating gates.

51. The method of claim 41, wherein each of the channel region first portions extends in a direction directly toward one of the floating gates.

52. The method of claim 41, wherein the formation of the floating gates includes forming a layer of the electrically conductive material before the formation of the trenches, and wherein the trenches are subsequently formed through portions of the layer of electrically conductive material.

53. The method of claim 41, further including the step of:

forming an indentation in a sidewall of each of the trenches so that the control gate first portion therein includes a protruding portion corresponding to the indentation that extends over and is insulated from a portion of one of the floating gates.

54. The method of claim 41, further including the step of:

forming an indentation in a sidewall of each of the trenches so that the control gate first portion formed therein includes a protruding portion corresponding to the indentation that extends over and is insulated from a first part of one of the channel region second portions, wherein one of the floating gates is disposed over and insulated from a second part of the one channel region second portion.

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55. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

a floating gate disposed over and insulated from a surface of the substrate; and

first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a non-linear channel region therebetween, wherein the channel region defines a path for programming the floating gate with electrons from the second region.

56. The device of claim 55, wherein at least a portion of the non-linearity of the channel region is defined within a plane that is substantially perpendicular to the substrate surface.

57. The device of claim 56, wherein the channel region has a first portion that extends in a direction from the second region directly toward the floating gate.

58. The device of claim 57, wherein the direction is substantially perpendicular to the substrate surface.

59. The device of claim 57, wherein the channel region has a second portion that extends in a direction from the channel region first portion to the first region.

60. The device of claim 56, wherein:

the channel region has a first portion that extends in a direction from the second region toward the surface of the substrate;

the channel region has a second portion that extends in a direction from the channel region first portion to the first region; and

the floating gate is disposed over and insulated from only a portion of the channel region second portion.

61. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

an electrically conductive control gate having a first portion formed in the substrate;

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first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a non-linear channel region therebetween, wherein the second region is formed underneath and is insulated from the control gate first portion, and the channel region includes a first portion that extends substantially along the control gate first portion and a second portion that extends substantially along a surface of the substrate; and

an electrically conductive floating gate disposed over and insulated from at least a portion of the channel region and a portion of the first region.

62. The device of claim 61, wherein the control gate has a second portion disposed over and insulated from the floating gate.

63. The device of claim 61, wherein the floating gate is disposed over the entire second portion of the channel region.

64. The device of claim 63, wherein channel region first portion extends in a direction directly toward the floating gate.

65. The device of claim 61, wherein the floating gate is disposed over only a portion of the channel region second portion.

66. A method of operating a semiconductor memory cell formed in a semiconductor substrate, the memory cell includes a substrate of semiconductor material of a first conductivity type, a floating gate disposed over and insulated from a surface of the substrate, and first and second spaced-apart regions formed in the substrate and having a second conductivity type, with a non-linear channel region therebetween, wherein the channel region defines a path for programming the floating gate with electrons from the second region, the method comprising the steps of:

coupling a positive voltage to the floating gate; and

inducing electrons to flow from the second region, through a first portion of the channel region, to inject electrons onto the floating gate.

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67. The device of claim 66, wherein channel region first portion extends in a direction directly toward the floating gate.

68. The device of claim 67, wherein channel region first portion extends in a direction substantially perpendicular to the substrate surface.

69. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type and having a surface;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions;

each of the active regions including a plurality of memory cells, wherein each of the memory cells includes an electrically conductive floating gate disposed over and insulated from the substrate surface;

a plurality of first regions formed in the substrate and having a second conductivity type, each of the first regions extends across the active regions in a second direction perpendicular to the first direction and is disposed at least partially underneath one of the floating gates in each of the active regions;

a plurality of second regions formed in the substrate and having the second conductivity type, each of the second regions extends across the active regions in the second direction and is disposed between a pair of the first regions, wherein the second regions are buried underneath the substrate surface; and

a plurality of electrically conductive control gates each extending along one of the active regions in the first direction.

70. The array of claim 69, wherein each of the control gates includes a plurality of first portions that are each disposed in the substrate and over one of the second regions.

71. The array of claim 70, wherein for each of the active regions, the control gate therein has a second portion that is disposed over and insulated from the floating gates.

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72. The array of claim 69, further comprising:

a plurality of channel regions in the substrate each extending between one of the first regions and one of the second regions.

73. The array of claim 72, wherein each of the channel regions has a first portion extending from one of the second regions toward the substrate surface, and a second portion extending substantially along the substrate surface.

74. The array of claim 69 wherein the second regions are integrally formed together in one of a plurality of conductive lines buried in the substrate, and wherein each of the conductive lines extends in the second direction and includes a raised portion that extends up to the substrate surface.